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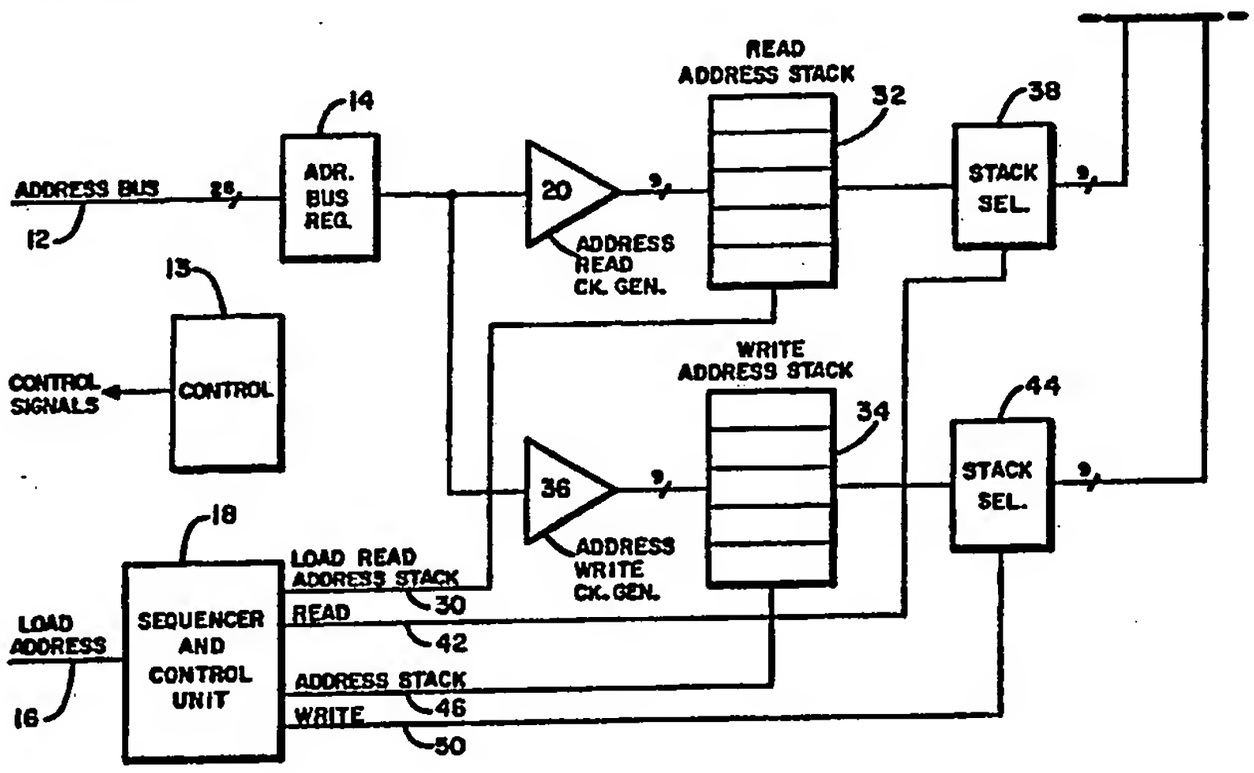
(54) Title: PIPELINED ADDRESS CHECK BIT STACK CONTROLLER



(57) Abstract

A memory system which is shared by a plurality of requestors each of which supply read and write address bits to the memory system is read out of, or written into, in accordance with read and write address bits. A sequencer is utilized to initiate a sequence of timing signals that control the reading, writing and partial writing of data. Certain ones of these signals occur at fixed intervals from the receipt of an initial load address signal. A read address circuit coupled to receive the read address bits generates a set of check bits. A read address stack means stores each set of read address check bits upon the occurrence of an associated load read address stack signal. A write address check bit generator means is coupled to receive write address bits and to generate a set of check bits representative of the write address bits. A write address stack means stores each set of the write address check bits upon the occurrence of an associated load write address stack signal. A read address stack selector and a write address stack selector read out read address check bits and write address check bits, while the sequencer controls the transmission of the read address check bits and the write address check bits to an error detection circuit.

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PIPELINED ADDRESS CHECK BIT STACK CONTROLLER

BACKGROUND OF THE INVENTION

Field of the Invention The present invention is related to the error checking and the detection of erroneous address bits in a data processing system, and, in particular, to error checking and detection of such address bit in a pipelined manner.

General Background Error checking and detection of bits for both data words and addresses is currently implemented in modern data processing systems. Such systems may require multiple ports to allow remote processors to access a common storage module. The present invention provides for single and double bit data and address error checking and for single bit error correction of the data bits in a pipelined manner with a minimum of overhead in terms of hardware and complexity.

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BRIEF DESCRIPTION OF THE DRAWINGS

The present invention is illustrated by reference to the drawing in which:

Fig. 1 shows a layout for Figs. 1a, 1b and 1c, and

Figs. 1a, 1b and 1c are an overall block diagram of the pipelined address check bit control system of the present invention.

TECHNICAL DESCRIPTION OF THE PREFERRED EMBODIMENT

A pipelined address check-bit stack controller constructed in accordance with the present invention is shown in the drawings. This controller is particularly useful in a multiple-user environment in which different requesters issue priority requests and the requestors are assigned priority on some predetermined basis. When an address has been sent by a remote requestor or processor (not shown) on the 26 bit Address Bus 12 to the Address Register 14, along with a Load Address signal from the Control Section 13 on the Load Address line 16 to the Sequencer 18, the address stored in the Address Bus Register 14 is coupled to a Address Read Check Generator 20. These 24 address bits may be used to specify memory units, banks, block addresses and words in an addressed block. The Address Read Check Generator 20 provides 8 check bits in a conventional manner to verify the integrity of the address information.

The Load Address signal on the line 16 initiates the timing cycle for the address check bit stacks and the loading of addresses. For simplicity of implementation, it is preferred that the Load Write Address Stack Pointer signal occurs at the same time as the Load Read Address Stack Pointer signal. The load address timing cycle begins upon a change of state of the Load Address signal

from a high to a low level. When a second load address request is received from the Control Section 13 and the Load Address signal again changes state from a high to a low, another new timing cycle is initiated. In a modern high speed data processing system these Load Address signals may occur as fast as every 30 nanoseconds.

The Load Read Register and Write Address Stack Pointers are advanced each time the Load Address signal goes from a high to a low level. This advancement occurs at a fixed, continuously repeatable sequence after each transition of the Load Address signal from a high to a low level. The Load Read Pointer signal is supplied on the line 30 to a Read Stack 32. This stack must be of sufficient depth to prevent overriding of stored information in the stack during normal operation, and generally will be of five levels or more. The Address Read Check Generator 20 produces 8 check bits that are stored in the Read Address Stack 32 that fill one level of the stack.

Although a single stack could be employed for both read and write operations, it is expedient for ease of implementation to supply a separate Write Address Stack 34, which is supplied 8 address write check bits from the Address Bus Register 14 through a separate Address Write Check Generator 36. This minimizes the number of different types of circuit chips that are required and provides duplexing which can be used to isolate errors that affect only one of the stacks.

During the read cycle, the first group of check bits that have entered into the Read Address Stack 32 emerge first from the stack. These check bits are supplied to the Read Stack Selector 38 which supplies 8 address check bits and a parity bit to an Exclusive-OR (XOR) Gate 40 under the control of the Read Pointer that is supplied by the Sequencer 18 on the line 42. In a similar manner, the Write Stack 34 receives 8 write check bits plus 1 parity bit from the Address Write Check Generator 36 under the control of the Load Write Pointer signal on the

line 46. The Write Stack Selector 44 is gated to one input of the Write Check Bit Generator 48 in response to the Write Pointer on the line 50 from the Sequencer 18. The check bits plus the associated parity bits from the Write Stack Selector 44 on its other input are used for write and partial write checking. The Write Check Bit Generator 48 generates 10 bits for each word of data, which consist of 8 check bits, a total data word parity bit and a parity bit for a byte formed of the 8 check bits and the total data word parity bit.

The read operation and the use of the stored Read Address Check Bits stored in the Read Address Stack 32 will now be discussed. The Read Bus 53 is 100 bits wide in the disclosed embodiment, and it is coupled to the Memory which has data, parity and check bits stored therein. The 100 bits consist of two data words of 36 bits (4 nine bit bytes) each, plus 1 total data word parity bit for each word, 8 check bits for each word, 4 data byte parity bits and one parity bit for a byte that consists of the 8 check bits and the total data word parity bit for each word.

These 100 bits are coupled into the Read Register 54 under control of signals from the Control Section 13 that are supplied on the Load Read Register Line 56. The 100 byte parity bits are checked at the interface by the Parity Check Circuit 55. Two words at a time, each consisting of 36 data bits plus 8 check bits and a total data parity bit are read out of the Read Register 54 to the Read Syndrome Generator 58, which generates 9 Read Syndrome bits. The output of the Read Syndrome Generator 58 is supplied to an error correction circuit 60 which may be of a type known in the art, to correct errors in the data word before it is sent to the Read Data Out Register 62 and the Read Data Register 64. Due to complexity of implementation, single and double bit error detection and single bit error correction of the data word should suffice for most applications. Two words of data plus the 8 data byte parity bits are stored in the

Data Read Out Register 62, and are read out on a selected port input line 66, 68, or 70 under the control of signals on the Load to Requestor Bus 72. The Read Data Register 64 is utilized when a Partial Write is performed, as will be described subsequently.

The Write operation precedes the Read operation, and, therefore, a Write Pointer signal on the line 50 occurs at an earlier time than the Read Pointer signal on the line 42. This is to allow for reading of data prior to its merging with write data in a partial write operation. Both the Write and Read Pointers occur at fixed intervals following the transition of the Load Address signal on the line 16 from a high to a low level after the start of each timing cycle of the Sequencer 18. During a Write cycle, the write data from the remote processor in control is transmitted in groups of two words of 72 data bits plus 8 data byte parity bits on the associated Write Buses 74, 76 or 78 to the Write Register 80 under control of the Load Write Register Line 82. The particular port write data that is to be written at any time is determined by the Port Select Decoder 84 as determined by code on the port selection Bus 86. The write data is then supplied to the Write Data Register 86. During a full word write, the Merge Select Register 88 receives two 36 data bit words plus 4 data byte parity bits. As previously noted, the Write Check Bit Generator 48 generates 20 check bits which are combined with data bits and stored in the Write Bus Register 90, and then these bits are transferred as 50 bit words for storage in the Memory 53.

Address check bits generated during Partial Write operations may also be verified with the pipelined address check bits stack controller of the present invention. A Partial Write operation results when a word which has been read from memory has been corrected, and then a predetermined number of bits are written over the corrected word. The portion of the word that is written over may be divided into partial word bits from 1 to 35

bits. Partial address write check bits are verified at the time subsequent to the time allotted for the verification of the read address bits.

When a Partial Write operation occurs, the word read from Memory 53 from the previous cycle is stored in the Read Data Register 64. The Start and End Code bits for controlling the Partial Write masking operation are supplied by each of the requestors on the Buses 92, 94, and 96 to the Start/End Register 98. There are 6 start bits plus a parity bit and 6 end bits plus another parity bit per merged word. The Port Selector Decoder 100 is responsive to the select signal on the line 86 to select 4 start/end and parity bits from one of the remote requestors. The selected Start and End Code bits from the requestor are then decoded and stored in the Start/End Merge Bit Register 102. A control signal from the Control Section 13 on the line 104 to the Start/End Merge Bit Register activates a Partial Write operation.

During a Partial Write operation, the Start/End Merge Bit Register 102 contains the code which specifies the Starting and Ending bits which specify where write data will overwrite a previously read data word. The write data is obtained from the remote requestors on the Buses 74, 76 and 78 via the Write Register 80, and the Port and Select Decoder 84 and the Write Data Register 86, as previously described in connection with the full write operation. The read data in the Read Data Register 64 and the write data in the Write Data Register 86 are then merged and stored in the Merge Select Register 88 in accordance with the decoded Start and End codes stored in the Start/End Merge Bit Register 102. Partial Write address check bits are gated out of the Write Stack Selector 44 by a Partial Write signal on the line 50 that occurs in time after the Read signal on line 42. The Write Address Stack 34 is thus able to accommodate the address check bits for both full Write and the Partial Write operations.

CLAIMS

1. A memory system which is shared by a plurality of requestors each of which is capable of supplying load address signals and read and write address bits to said memory system, comprising a memory means which is read out of, or written into, in accordance with the binary values of said read and write address bits in either a Read, a Write or a Partial Write mode,

sequencer means for initiating a series of timing signals upon receipt of said load address signals comprising the sequence of write signals, read signals and partial write signals, each of which signals occur at a fixed interval from the receipt of each of said load address signals,

read address means coupled to receive said read address bits for generating a set of check bits representative thereof,

read address stack means for storing each set of said read address check bits upon the occurrence of an associated read signal,

write address check bit generator means coupled to receive said write address check bits for generating a set of check bits representative thereof,

address stack means for storing each set of said address check bits upon the occurrence of an associated write signal,

error detection means, and

address stack selector means for reading out said address check bits from said address stack means to said error detection means,

wherein said sequencer means controls the timing of said read address check bits and said write address check bits to said error detection and correction means so as to either provide read address, write address or partial write address error detection in accordance with

whether said memory system is performing a Read, a Write or a Partial Write operation.

2. A memory system as claimed in claim 1 wherein said write signals occur prior to said read signals which in turn occur prior to said partial write signals in a fixed repetitive time sequence.

3. A memory system which is shared by a plurality of requestors each of which is capable of supplying read and write address bits to said memory system, comprising memory means which is read out of, or written into, in accordance with the binary values of said read and write address bits in either a Read, a Write or a Partial write mode,

sequencer means for initiating a series of timing signals upon receipt of said load address signals comprising a sequence of write signals, read signals and partial write signals, each of which signals occur at a fixed interval from the receipt of each of said load address signals,

read address means coupled to receive said read address bits for generating a set of check bits representative thereof,

read address stack means for storing each set of said read address check bits upon the occurrence of an associated read signal,

write address check bit generator means coupled to receive said write address bits for generating a set of check bits representative thereof,

write address stack means for storing each set of said write address check bits upon the occurrence of an associated write signal,

error detection means,

read address stack selector means for reading out said read address check bits from said read address stack means to said error detection and correction means, and

write address stack selector means for reading out said write address check bits from said write address

stack means to said error detection and correction means,

wherein said sequencer means controls the timing of said read address check bits and said write address check bits to said error detection and correction means so as to either provide read address, write address or partial write address error detection in accordance with whether said memory system is performing a Read, a Write or a Partial Write operation.

4. A memory system as claimed in claim 3 wherein said write signals occur prior to said read signals which in turn occur prior to said partial write signals in a fixed repetitive time sequence.

5. A method of operating a memory system which is shared by a plurality of requestors each of which is capable of supplying load address signals and read and write address bits to said memory system, comprising initiating a series of timing signals upon receipt of said load address signals comprising the sequence of write signals, read signals and partial write signals, each of which occur as a fixed interval from the receipt of each of said load address signals,

generating a set of check bits representative of said read address bits,

storing each set of said read address check bits,

generating a set of check bits representative of said write address bits,

storing each set of said write address check bits,

performing error detection of said read and write address bits, said read and write address check bits so as to either provide read address, write address or partial write address error detection in accordance with whether said memory system is performing a Read, a Write or a Partial Write operation.

6. A method as claimed in claim 5 wherein said write signals occur prior to said read signals which in

turn occur prior to said partial write signals in a fixed repetitive time sequence.

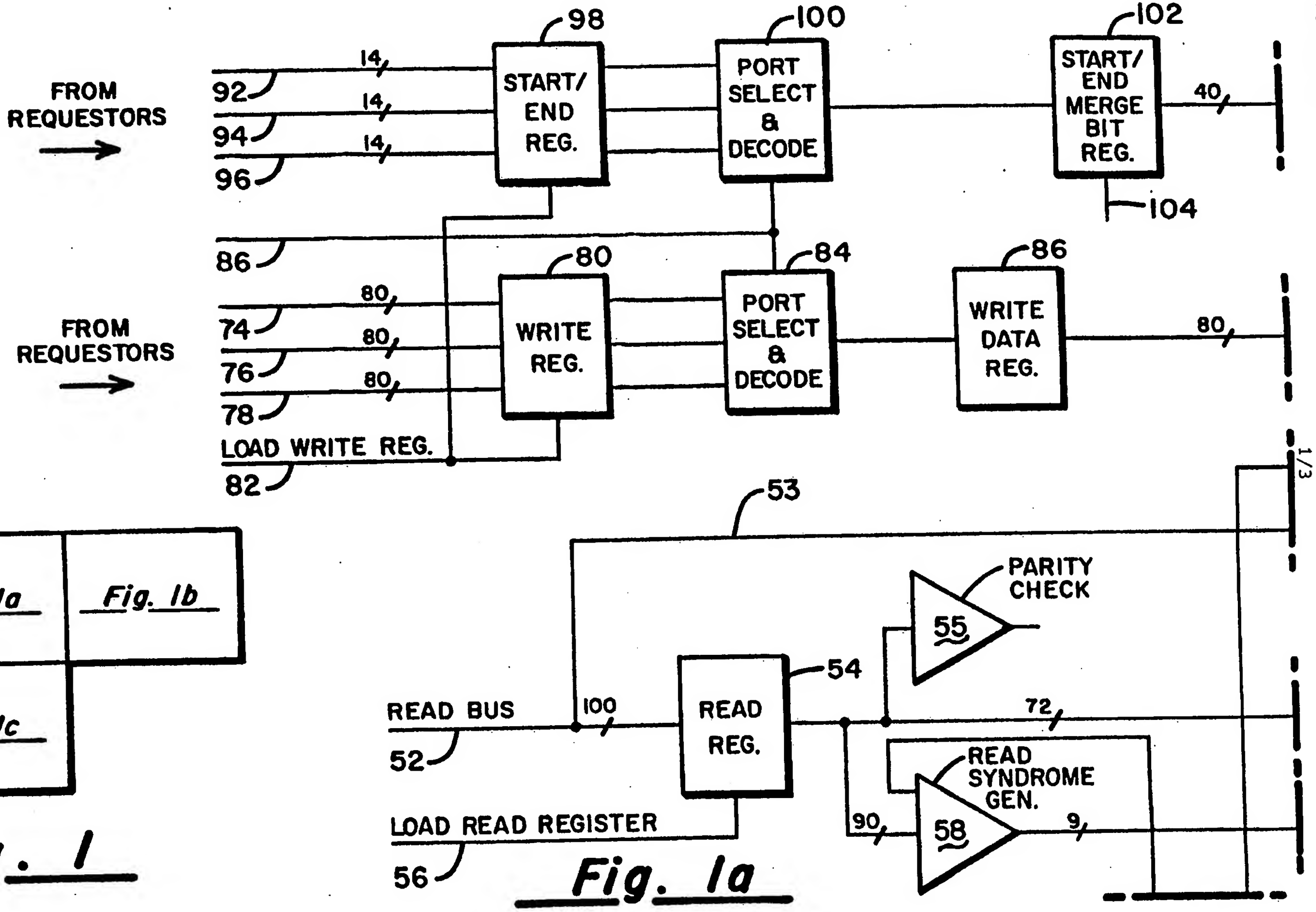
FROM REQUESTORS
92
94
96
14
14
14
98
START/ END REG.
100
PORT SELECT & DECODE
102
START/ END MERGE BIT REG.
40
104
86
FROM REQUESTORS
74
76
78
80
80
80
80
WRITE REG.
84
PORT SELECT & DECODE
86
WRITE DATA REG.
80
LOAD WRITE REG.
82
1/3
53
PARITY CHECK
55
READ BUS
52
100
READ REG.
54
72
READ SYNDROME GEN.
90
58
9
LOAD READ REGISTER
56

Fig. 1a

Fig. 1

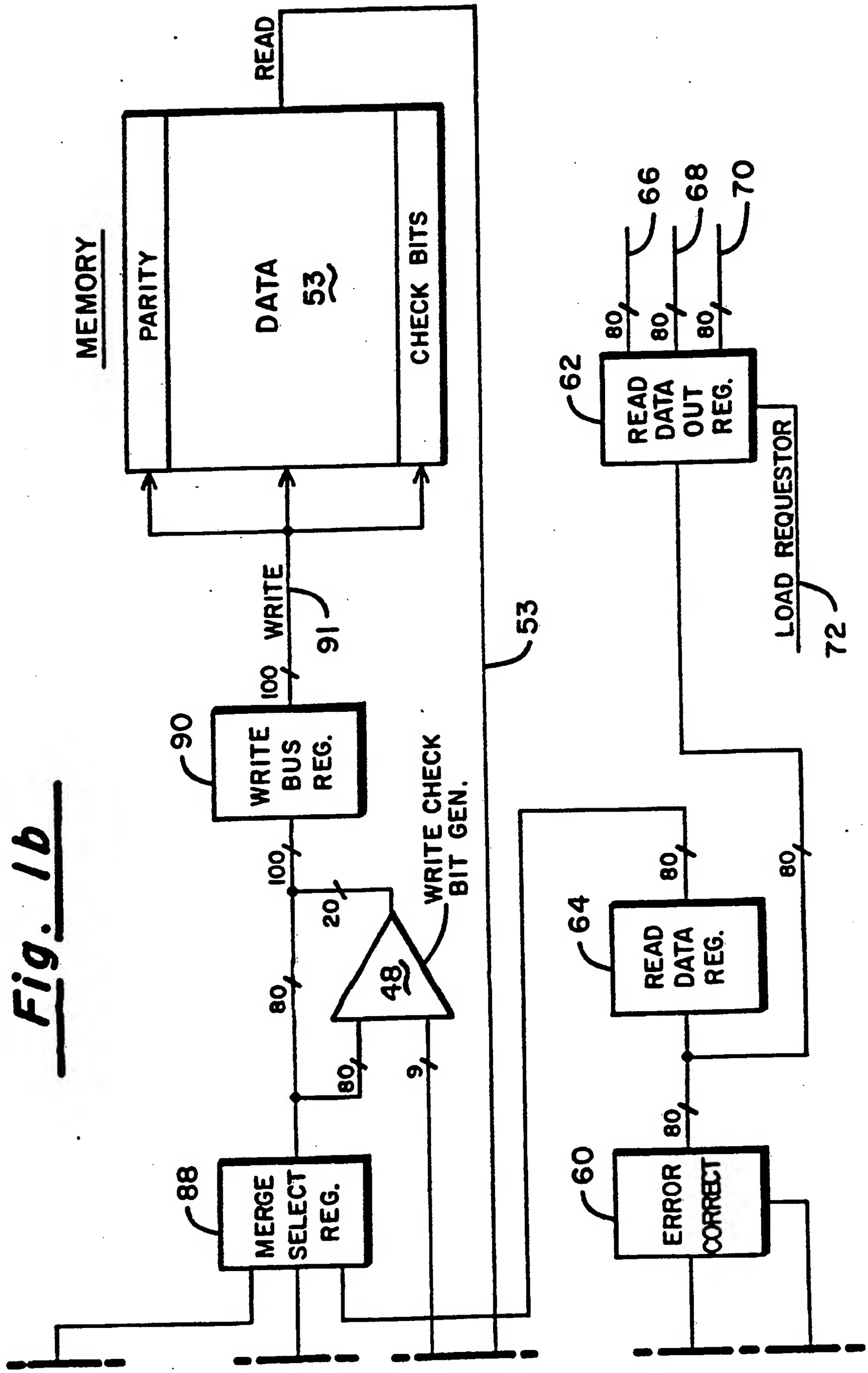
MEMORY
PARITY
DATA
53
CHECK BITS
READ
66
68
70
80
62
READ DATA OUT REG.
LOAD REQUESTOR
72
53
WRITE
100
91
90
WRITE BUS REG.
100
WRITE CHECK BIT GEN.
20
48
80
9
64
READ DATA REG.
88
MERGE SELECT REG.
60
ERROR CORRECT

Fig. 1b

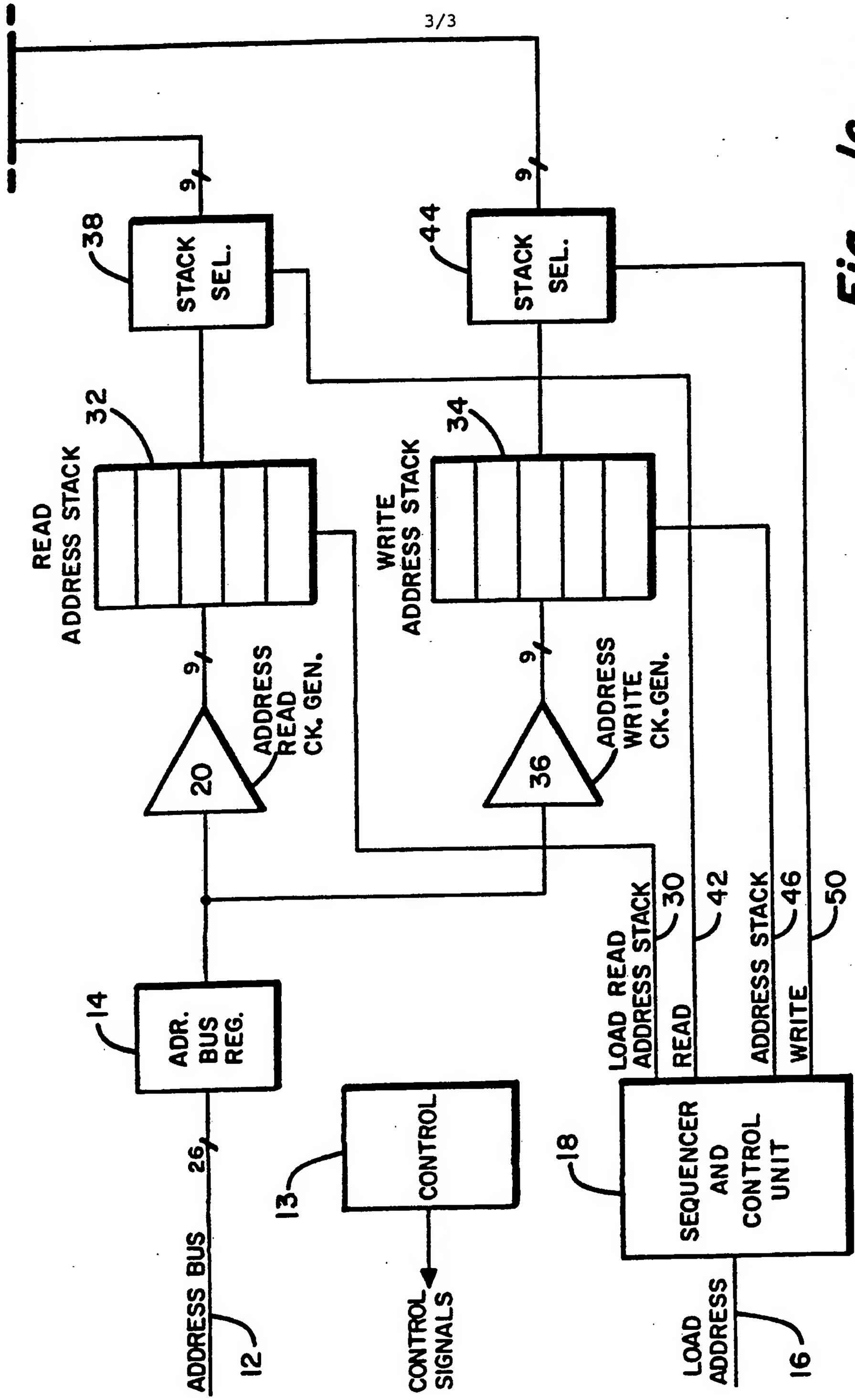
9
9
38
STACK SEL.
44
STACK SEL.
32
READ ADDRESS STACK
34
WRITE ADDRESS STACK
9
9
20
ADDRESS READ CK. GEN.
36
ADDRESS WRITE CK.GEN.
30
42
46
50
LOAD READ ADDRESS STACK
READ
ADDRESS STACK
WRITE
14
ADR. BUS REG.
26
ADDRESS BUS
12
13
CONTROL
CONTROL SIGNALS
18
SEQUENCER AND CONTROL UNIT
LOAD ADDRESS
16

Fig. 1c

INTERNATIONAL SEARCH REPORT

International Application No PCT/US 89/03523

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all) [6]

According to International Patent Classification (IPC) or to both National Classification and IPC

IPC[5]: G 06 F 11/10

II. FIELDS SEARCHED

Minimum Documentation Searched [7]

Classification System	Classification Symbols
IPC[5]	G 06 F 11/10

Documentation Searched other than Minimum Documentation to the Extent that such Documents are included in the Fields Searched [8]

III. DOCUMENTS CONSIDERED TO BE RELEVANT [9]

Category *	Citation of Document, [11] with indication, where appropriate, of the relevant passages [12]	Relevant to Claim No. [13]
A	US, A, 3963908 (DAS) 15 June 1976 see abstract; column 3, line 1 - column 4, line 20, claims 1,5 --	1,3,5
A	Patent Abstracts of Japan, volume 4, no. 172 (P-38)(654), 27 November 1980, & JP, A, 55117799 (HITACHI SEISAKUSHO K.K.) 10 September 1980 see the whole abstract --	1,3,5
A	Electronic Design, volume 29, no. 20, 30 September 1981, (Waseca, MN, US), M. Bazes et al.: "Keep memory design simple yet cull single-bit errors", pages 195-201 see page 195, right-hand column, line 18 - page 201, right-hand column, line 2 --	1,3,5
A	US, A, 4174537 (CHU et al.) 13 November 1979 -- ./.	

* Special categories of cited documents: [10]

"A" document defining the general state of the art which is not considered to be of particular relevance

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"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

IV. CERTIFICATION

Date of the Actual Completion of the International Search	Date of Mailing of this International Search Report
21st November 1989	13. 12. 89
International Searching Authority	**Signature of Authorized Officer**
EUROPEAN PATENT OFFICE	T.K. WILLIS

International Application No. PCT/US 89/03523

III. DOCUMENTS CONSIDERED TO BE RELEVANT (CONTINUED FROM THE SECOND SHEET)

Category *	Citation of Document, with indication, where appropriate, of the relevant passages	Relevant to Claim No
A	US, A, 4253147 (MacDOUGALL et al.) 24 February 1981	

ANNEX TO THE INTERNATIONAL SEARCH REPORT ON INTERNATIONAL PATENT APPLICATION NO. US 8903523 SA 30687

This annex lists the patent family members relating to the patent documents cited in the above-mentioned international search report.
The members are as contained in the European Patent Office EDP file on 06/12/89
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Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US-A- 3963908	15-06-76	CA-A- 1060123	07-08-79
US-A- 4174537	13-11-79	US-A- 4138720	06-02-79
		US-A- 4371949	01-02-83
US-A- 4253147	24-02-81	None	